A flexible compact readout circuit for SPAD arrays

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ABSTRACT

A compact readout circuit that can be integrated between individual single photon avalanche detectors (SPADs) is described. The circuit uses minimum sized transistors to both quench the avalanche process in the photodetector and integrate charge onto a capacitor to represent the number of detected photons. An additional transistor is integrated within the circuit so that the integration capacitance can be isolated from the source-follower output circuit before the integration time has elapsed. This device can be used by the user to control the relationship between the number of detected photons and the output voltage.

Keywords: SPAD, Imaging, pixel

1. INTRODUCTION

A single photon avalanche detector (SPAD) is a sensitive photodetector whose high gain arises from avalanching within a photodiode. An array of SPADs could form a sensitive imaging sensor and several groups have created SPAD arrays in a single silicon substrate using commercial CMOS technologies. For example a two dimensional array of 32 by 32 SPADs has been reported [1], however a lack off in-pixel storage meant that an external digital counter was required. Alternatively, in-pixel digital counters have been reported [2, 3] however the digital counter and peripheral circuits are relatively large compared to the photodiode. This limits the density of the SPAD array. To achieve a denser array of SPADs, a small and compact SPAD pixel is proposed in this paper. A SPAD has been implemented in a UMC 0.18µm 1P6M Triple-Well process. A flexible analogue circuit is proposed that can be implemented in the free space between the circular photodetectors that the critical part of each SPAD. This analogue circuit has been designed so that the user can control its response using an input voltage. Results are presented that show that using this voltage it is possible to have a linear or a dual slope linear response. It is expected that in the future it will be possible to create other responses, including a wide dynamic range logarithmic response.

2. THE SPAD

2.1 Operation

A SPAD is based upon a photodiode which is biased over its avalanche breakdown voltage. When a conventional photodiode is manufactured in a planar fabrication technology, a layout is used that contains edges and corners. At the near zero operating voltages of conventional photodiodes these edges and corners are irrelevant. However, at the higher operating voltages used in a SPAD the electrical field enhancement at these edges and corners cause premature breakdown in these regions. To prevent premature breakdown the electrical field at the edges of the photodiode within a SPAD must be reduced by using a low doped material as a guard ring. Fig [1] shows the cross section of a SPAD photodiode fabricated in CMOS 0.18µm Triple-well technology. For the photodiodes that have been tested the 10µm diameter p+/N-well junction that forms the active area of the device is surrounded by a P-Well guard ring. A deep N-well layer then provides an electrical connection to N-well part of the active area and the device is circular to avoid any corners. Results such as those in Fig [2] show that these devices have a breakdown voltage of 10.4 volts.

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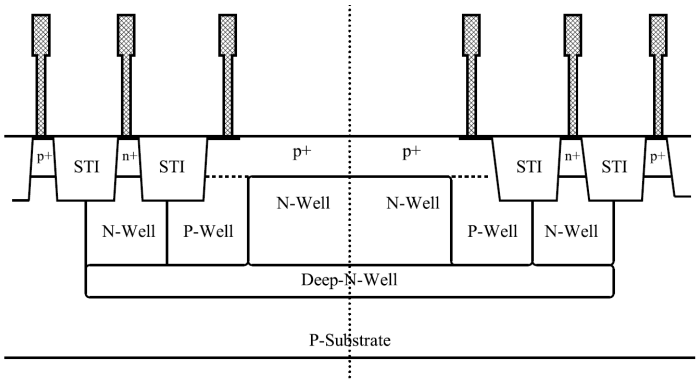

Figure 1.A cross section through the SPAD

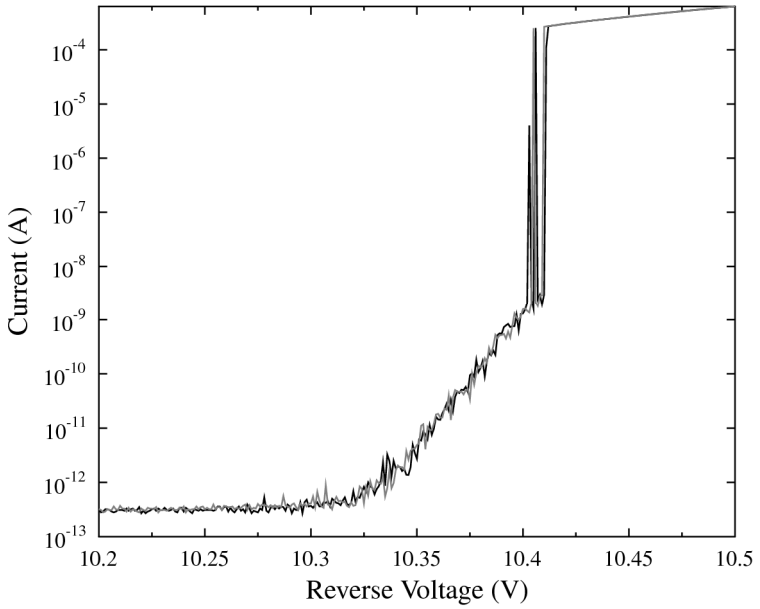

Figure 2. Two measured I-V curves for a typical fabricated SPAD showing that avalanche breakdown occurs around 10.4V.

2.2 Dark Count and PDP

Since the photodiode is biased at a voltage above its avalanche breakdown voltage any electron-hole pair arising within the photodiode will create a charge pulse that will be self-sustained unless the voltage across the photodiode is reduced below the avalanche breakdown voltage. The process of reducing the voltage across the photodiode when a charge pulse occurs is known as quenching. The quenching mechanism that has been adopted in the circuits that have been designed and tested is passive quenching based upon a pMOS device connected in series with the photodiode. In this configuration

the gate voltage of the pMOS quenching device determines the recovery time after a charge pulse. The change in photodiode voltage caused by a charge pulse is then converted to a digital signal using an inverter [1, 4].

When the SPAD is operated in the dark spontaneous pair generation means that charge pulses will occur despite the absence of light. The rate of pulse generation in the dark is referred to as the Dark Count Rate (DCR). The DCR depends upon factors including the layout of the photodiode and the doping concentrations in the photodiode. In CMOS technologies with critical dimensions less than 0.25µm the high doping concentrations mean that tunnelling also contribution to the dark current [5]. Fig [3.A] shows the relation between the DCR and the over voltage for the devices that have been tested. These results show that as expected the dark count rate increases rapidly as the overvoltage is increased.

To measure the light response of the SPAD a green LED, with a peak wavelength of 570nm and FWHM of 25nm, was installed at the entrance port of an integrating sphere to form a uniform illumination at the exit port. The relationship between the voltage applied to the LED and the intensity of the beam from the exit port was then obtained using a JAZZ Spectrometer. Using this method the system was calibrated to light levels as low as 100µlx. The sample was then placed a few millimetres from the exit port in an enclosed metal box. To determine the Photon Detection Probability the number of pulses from the inverter output was then counted. The difference between the average count at approximately 1.1lux and the average dark count in the same period was then calculated. The ratio between this difference and the number of incident photons expected in the time period was then used to determine the Photon Detection Probability (PDP). The results in Fig [3.B] show the changes to the PDP as the over voltage is varied. These results show that the PDP increases with over voltage, however it saturates at higher voltage level.

The choice of the operating over voltage is an import parameter in SPAD operation. As Fig [3] shows that the Dark Count Rate and PDP both increase as the over voltage increases, but at different rates and the PDP saturates at higher over voltages. This suggests that there is an optimum over voltage. To determine the optimum over voltage the Signal-to-Noise Ratio of the SPAD has been defined as the ratio between average light count and the standard deviation of the total number of counts (light and dark) in the16ms integration time. Since both the incident photons and the dark counts have a Poisson distribution the standard deviation of the total number of counts is equal to the square root of the overall counts. Fig [4] shows the calculated SNR in various over voltages. These results suggest that for this integration time an over voltage 1.2V has the highest SNR and is therefore the best biasing condition for the photodiode.

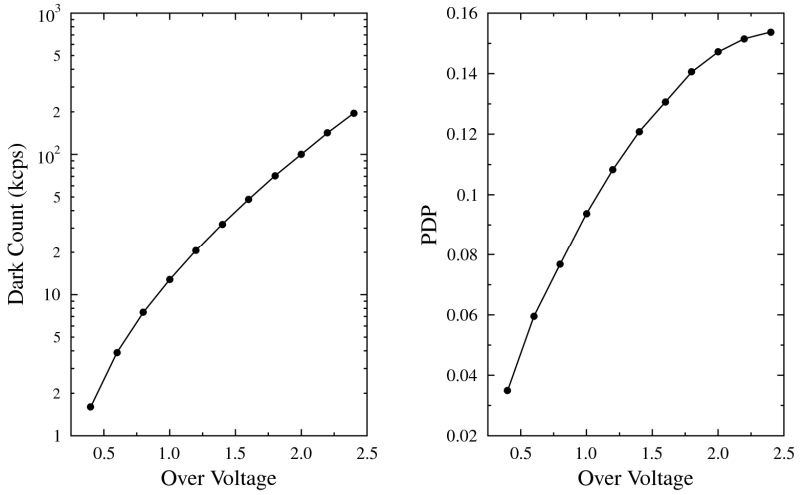

Figure 3. (A) Dark Count Rate of the SPAD, and (B) Photon Detection Probability at λ=570nm versus over voltage and illumination 1.1 lux

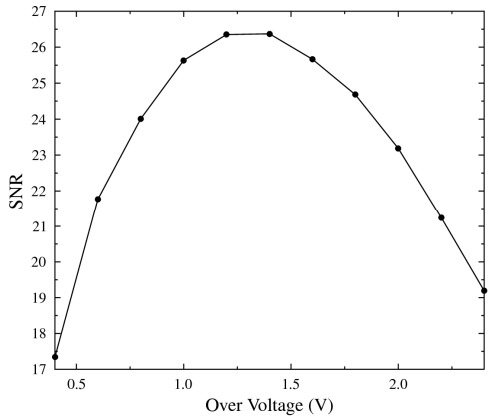

Figure 4. The SNR at 1.1 lux for a 16ms integration time versus over voltage. The peak SNR occurs about 1.2 volt of over voltage

3. PIXEL

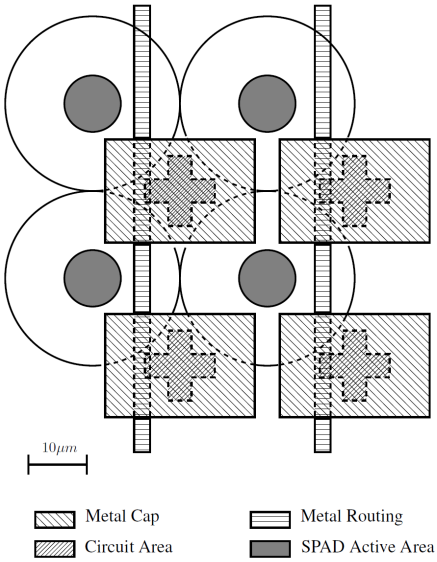

Figure 5. Floor plan of a two dimensional array of SPADs and associated circuits. The large circles are the photodiodes which consist of a central active area surrounded by a large guard ring with a diameter of 30 μm.

The conventional approach to counting the number of photons detected by a SPAD in a particular time period is to use a digital counter. However, in a two dimensional array, a high density of pixels may not be achieved due to relatively large area of a digital counter. The alternative approach to counting photons that has been investigated is to use an analogue circuit. A schematic diagram of the proposed pixel circuit is shown in Fig [6]. All the transistors are thick gate devices and have a minimum geometry (L=340nm and W=240nm) except the quenching transistor, Mq, which is 1μm long and 240nm wide. The storage capacitor, C_{MIM}, which is approximately 400fF, has been implemented as a Metal-Insulator-Metal capacitor using the top two levels of metal. The gate of quenching transistor Mq, can be controlled by an external bias voltage V_{SPAD} to vary the recovery time. In practice due to the high resistance of Mq, this gate was connected to ground to give the minimum recovery time. The photodiode bias voltage is determined by both VPOS, a positive

voltage, and VNEG, a negative voltage. To achieve the optimum signal to noise ratio in 16ms the SPAD is operated with an over voltage of 1.2V. When a photon is detected, the SPAD voltage across the photodiode drops until its overvoltage is zero. Once avalanching is quenched the voltage is then increased by the current provided by Mq. The SPAD node is connected to a digital inverter which amplifies the changes in the SPAD node voltage. This also means that transistor M_s only conducts whilst the photodiode is recovering from a charge pulse and is therefore only conducting for a short period of time t_{ON}. This time depends on recovery time of the SPAD, and threshold voltage of the inverter. Although the threshold voltage of the inverter is determined during the design stage and is then fixed, the SPAD biasing voltages VPOS and VNEG can be varied to change the relationship between the voltage swing at the SPAD node and the threshold voltage of the inverter. The SPAD biasing voltages have been chosen so that the threshold voltage of the inverter is half way between the maximum and minimum SPAD node voltages. When M_s is conducting the current flowing through transistor M_d discharges C_{MIM}. At the beginning of each integration time C_{MIM} is reset to VDD by the reset pulse. Every incident photon then removes a small charge from C_{MIM}. If M_d acts as a constant current source, then the change in the voltage on C_{MIM} during a time interval t_{int} is proportionate to the number of photons detected in this time interval. If the gate of M_{iso} is grounded, so that this device is always conducting, then the voltage on C_{MIM} can be detected using the source follower circuit. This n-type source follower has a SEL switch to enable its output and a biasing transistor M_b, whose gate voltage is set to 1.0V during experiments.

3.1 Linear Mode

Fig [7] shows the output voltage of the pixel when it is operated in this linear mode with the gate voltage of M_d set to 0.68V so that each photon discharges C_{MIM} by approximately 140mV. Using this bias condition it is easy to see the effect of each photon on the pixel. However, with a limited voltage swing of 2V only 14 photons can be detected with this bias condition. Assuming that the output voltage will be sampled using an analogue to digital converter then during normal operation V_{dis} should be set so that each photon causes a voltage change that is equivalent to a change on 1 bit in the ADC output. With a 10 bit ADC this means that V_{dis} was set so that each photon discharged C_{MIM} by approximately 2mV. Fig [8] shows the response of the pixel at different light levels when the integration time of the pixel is set to 16ms. The dark count rate of the SPAD means that the average dark count in this period is approximately 450 counts. Hence, the measured output voltage of the pixel in the dark is approximately 1.1V. The results in Fig [8] show that at low light levels the response of the pixel is linear as expected. However, there is a clear departure from linearity when the light intensity is more than 1lux. Measurement and simulation results show that this departure from linearity arises because transistor M_d is not an ideal constant current source. The linearity of the pixel can therefore be improved by making this device longer in future designs.

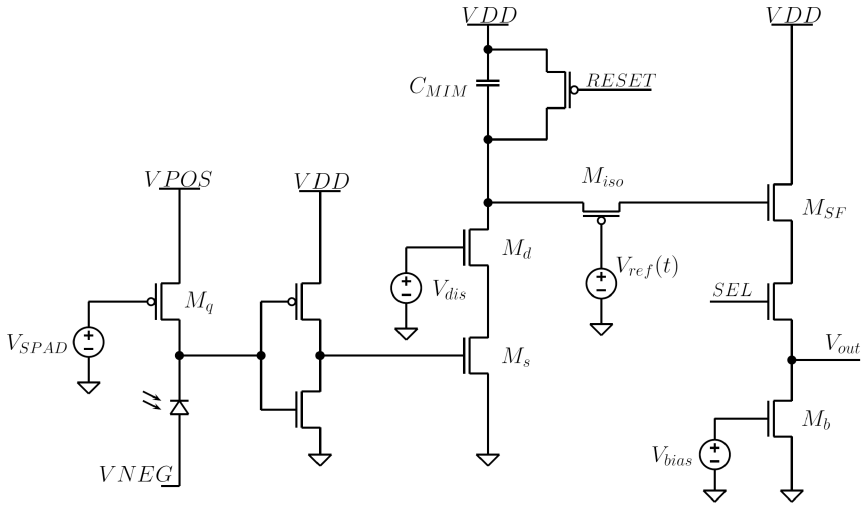

Figure 6. A schematic diagram of the pixel circuit. The photodiode and quenching device are on the left. These devices are connected to the rest of the circuit by an inverter.

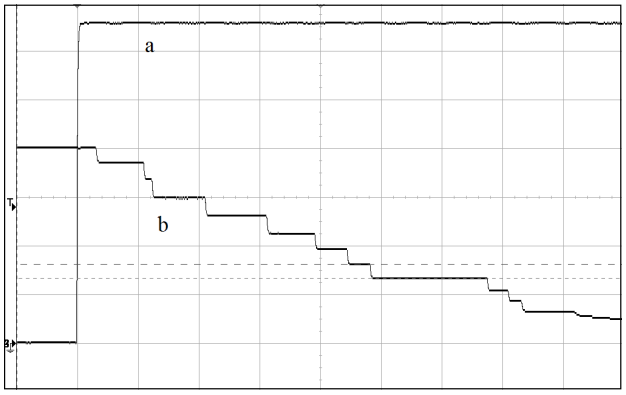

Figure 7. Discharging of linear mode operation when step size is about 140mV. (a) the reset pulse (b) the output voltage (500mV, 50µs per division)

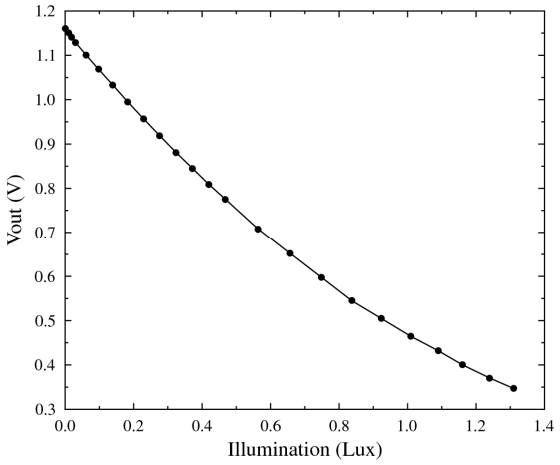

Figure 8. The output voltage of the pixel versus illumination when operating in linear mode.

3.2 Isolation Mode

In the linear mode of operation the gate of transistor M_{iso} is grounded and this device is therefore always conducting. This device will only conduct whilst $V_{cap} > V_{ref} + V_{th}$ and hence by changing the user generated input voltage V_{ref} it is possible to isolate the source-follower output circuit from C_{MIM}. Since the condition for isolation depends upon the circuit's response and the user defined reference voltage this mechanism allows the user to create an input dependant effective integration time. Previously this method has been used to create a wide dynamic range logarithmic response in conventional CMOS pixels [6].

The circuit in Fig [6] has been tested using the time dependant reference voltage, $V_{ref}(t)$, which had previously been used to obtain a wide dynamic range logarithmic response from CMOS pixels. Results such as those in Fig[9] show that as expected this creates a pixel with a wider input dynamic range in a smaller range of output voltages. Equally clearly the response is not the expected logarithmic response.

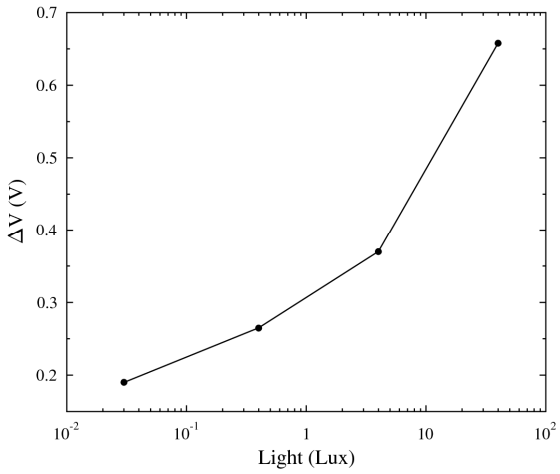

Figure 9. Output voltage of the pixel in Vref mode versus illumination with a logarithmic Vref(t) input The dynamic range of the light is limited by the light source used and not the voltage range.

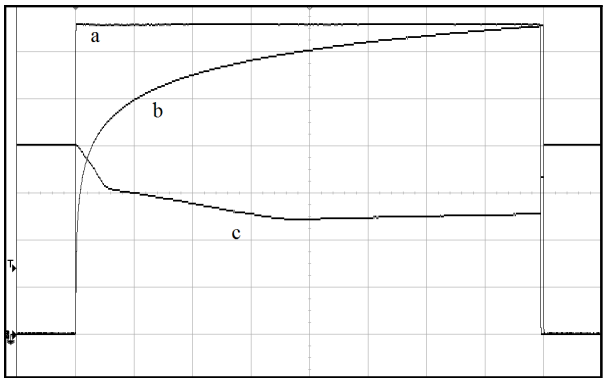

Figure 10. operation of the pixel during integration time in constant Vref mode with a logarithmic reference voltage (a) reset pulse, (b) logarithmic time dependent Vref, (c) pixel output (500mV, 2ms per division)

To investigate the unexpected results in Fig[9] the response of the pixels has been investigated during an integration period. Fig [10] shows the reset pulse that defines the integration period and the reference voltage that was expected to create a logarithmic response. The expected response of the output of the pixel to this input reference voltage is that this voltage should decrease linearly as C_{MIM} is discharged until the pixel output is isolated from C_{MIM}. Once the output is isolated the output voltage should be constant. The results in Fig [10] show the initial expected decrease in the output voltage which is caused by the discharge of C_{MIM} and a later period during which the output is almost constant. However between these two periods there is an unexpected period during which the output voltage decreases but at a slower rate than during the initial period.

The origin of the unexpected phase of the pixel response has been investigated by holding the reference voltage at different constant values. Fig[11] shows the pixel output when the reference voltage is 0V or 2V, so that the response of the pixel when the output is isolated can be compared to the response when the output is never isolated. As expected when the M_{iso} is always conducting the output voltage decreases as C_{MIM} is discharged. This decrease in the output voltage stops once the voltage on the input of the source-follower is less than the minimum input to the source-follower, which is 1V. When the reference voltage is 2V, so that the source-follower becomes isolated, the initial decrease in the output voltage is identical to the previous results. Again this is followed by a period during which the output voltage decreases at a slower rate. Taking into account the limitation on the minimum input voltage to the source-follower it is clear that this unexpected period ends once C_{MIM} is completely discharged. A review of the pixel layout shows that the

lower of the two metal layers in C_{MIM} is the one whose voltage varies. This means that there is a coupling capacitance between this varying voltage and the isolated source-follower input. It is this coupling capacitor which means that the output voltage continues to change after isolation until C_{MIM} is fully discharged. The coupling between C_{MIM} and the source-follower input means that the rate of change of the output voltage after isolation is approximately 11 times slower than the rate of change before isolation.

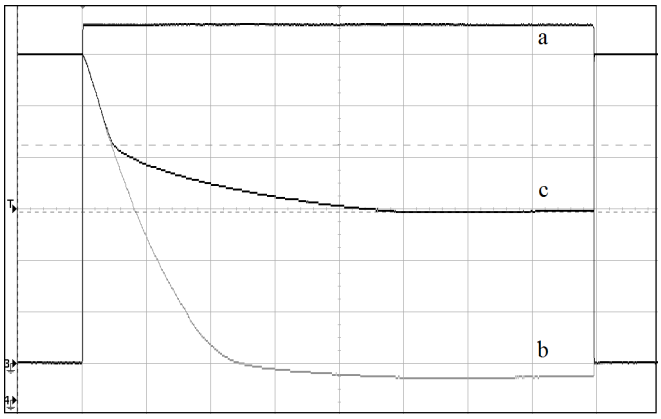

Figure 11. operation of the pixel in dual-slope mode during integration time (Vref=2.0, illumination=2lux) (a) reset pulse, (b) pixel output when Vref=0, (c) pixel output when Vref=2.0, (a: 500mV, b:300mV, 2ms per division)

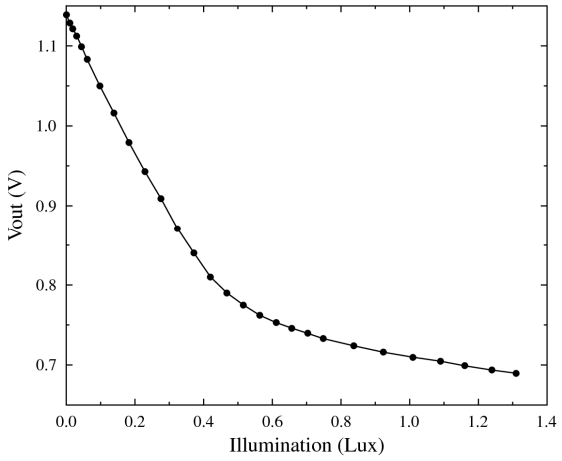

Figure 12. Output voltage of the pixel in dual-slope mode versus illumination (Vref=0.9V)

The coupling between C_{MIM} and the source-follower input creates an opportunity for the user to force the pixel to have a piece-wise linear response. This response can be obtained using a constant input voltage on the gate of M_{iso} which is chosen so that the source-follower will be isolated for part of the integration period. Fig[12] shows the output voltage when this voltage is chosen so that isolation occurs when the illumination is brighter than 0.5lux. As expected this creates a response which has two linear regions, the gradients of the two regions are 0.78 V/lux, and 0.07 V/lux. A comparison of the results in Fig[12] with those in Fig[8] shows that the result of the reduced gradient over part of the illumination range is that the pixel will have an increased dynamic range. In particular when the pixel is operated in its linear mode the maximum illumination level before the output voltage change saturates is approximately 1.5 lux. In

contrast when the reference voltage is chosen so that the source-follower is isolated immediately the maximum detectable illumination will be approximately 20lux. An even larger increase in dynamic range will be possible once the effect of the capacitive coupling between C_{MIM} and the source-follower have been included in the model used to calculate the $V_{ref}(t)$ needed to obtain a logarithmic response.

4. CONCLUSION

A compact readout circuit that can be integrated between individual circular SPADs has been described. The circuit converts the output pulses from the SPAD into charge pulses that discharge a capacitance. This mechanism means that the output voltage of the circuit is ideally proportional to the number of detected photons. The sensitivity of the circuit can be varied using a bias voltage that controls the charge pulse created by each photon. The circuit also contains a transistor that can be used isolate the SPAD from the source-follower output circuit. This transistor has been designed to allow the user to control the response of the circuit so that the user can increase the dynamic range of the circuit whilst maintaining a high sensitivity at low light levels. This transistor has been used to create a dual slope linear response. In the future it will be possible to create other responses, including a logarithmic response.

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